REMARKS/ARGUMENTS

The Applicant respectfully requests further examination and reconsideration in view of the comments set forth fully below. Claims 1-3, 5, 8, 9, and 37-39 were pending. Within the Office Action, Claims 1-3, 8, 9, and 37-39 have been rejected. By the above amendment, Claim 39 has been amended. Accordingly, Claims 1-3, 5, 8, 9, and 37-39 are now pending in the application.

Priority Claim

Within the Office Action, it is noted that the priority document does not adequately support the claims as required by 35 U.S.C. § 112. Within the specification, the priority document serial number contains a typographical error. By the concurrently filed Petition, Statements and original copy of the priority document pursuant to 37 C.F.R. §1.78(a)(6), the Applicants have corrected the priority. A typographical error was made in the original specification that pointed to the incorrect priority document. Specifically, the priority document serial number was recorded as 60/460,492 when it should have been 60/460,495. The original priority document is identical to the application as originally filed, and therefore fully supports the Claims.

Rejections Under 35 U.S.C. § 112:

Within the Office Action, Claim 39 is rejected under 35 USC 112 as failing to point out and distinctly claim the subject matter which applicant regards as the invention. By the above amendment, the Applicants have clarified the scope of the claim. Support for the Claim can be found in Claim 27 of the original application, and support regarding testing the integrated circuit can be found at least on Page 6, Lines 21-25.

Rejections Under 35 U.S.C. §103:

Within the Office action, Claims 1-3, 8, 9, and 37-39 have been rejected as being unpatentable over US Patent Application No. 2004/0116096 to Shen (Hereinafter Shen) in view of US Patent No. 7,715,815 to Gomez (Hereinafter Gomez) and further in view of US Patent Pub. No. 2006/0209987 to Miyagi (Hereinafter Miyagi) and further in view of US Patent Pub. No. 2003/0193373 to McCarthy (Hereinafter McCarthy). Applicants respectfully disagree.

Prior Art

Gomez and Miyagi are not prior art. With the concurrently filed Petition and supporting documents, the Applicants have perfected the priority date of April 3, 2003 for the present application. Specifically, Gomez has a priority date of May 2003. As a result, Gomez is not available under 35 U.S.C. § 102 to form the basis of a rejection under 35 U.S.C. §103. Miyagi is an international application that has a PCT filing date of July 30, 2003. Applications filed after Nov. 29, 2000 must have a PCT filing date before the filing date of the instant application in order to be considered prior art. For prior art purposes, the US filing date of Miyagi is no earlier than its PCT filing date, July 30, 2003 [MPEP 2136.03(II)] which is later than the April 3, 2003 filing date of the present application.

Shen teaches an RF communications receiver which permits greater integration on standard silicon chips and consumes less power than previous receivers. Also, Shen teaches a new method for using a tracking polyphase filter for image rejection of variable intermediate frequencies, wherein the method allows for reduced sensitivity to resistor and capacitor manufacturing variations and allows for the polyphase filter response to be enhanced compared to the prior art. [Shen, Abstract]

McCarthy teaches a programmable capacitive network for use in a tunable resonant circuit that is particularly useful in the tuning of a voltage controlled oscillator formed on a substrate, such as a semiconductor substrate or the like. The programmable capacitive network includes a plurality of capacitive elements. An interconnected network of voltage gate elements and fuse elements are interconnected with the capacitive elements to selectively connect one or more of the plurality of capacitive elements in the resonant circuit in response to at least one program control signal. In accordance with one embodiment, the voltage gate elements are diodes. [McCarthy, Abstract]

As admitted to in the Office Action, neither Shen, nor McCarthy, nor their combination teaches an intermediate frequency filter for use in an integrated circuit comprising the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface. Furthermore, neither Shen, McCarthy nor their combination teaches an intermediate frequency filter (IF filter), the IF filter including a first filter stage, the first filter stage including a first LC resonator; the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of fuses, wherein the first plurality of fuses programmable through the serial control module.

McCarthy teaches fuses that are self setting according to a voltage drops across diodes

(155-180 of Figure 1A) that cause the diodes to be forward biased and conduct across fuses (185-190) that are blown. In fact, McCarthy teaches away from the use of serial control and discusses several means and methods for automatic control of the fuses:

> There are a variety of methods that the automatic tuning unit 193 may use to determine the appropriate level for the programming signal. For example, the raw frequency value of the output from the frequency generator 105 may be directly compared to a lookup table or otherwise used in a quantitative calculation to generate programming signal. Alternatively, the raw frequency value may be compared to the output of a frequency generator 195. The difference between the VCO output signal frequency and the frequency of the signal provided by the standard frequency generator 195 may be used by the automatic tuning unit 193 for comparison with a lookup table or use in a quantitative calculation. Still further, this difference may be used in a closed-loop analog feedback system. It will be recognized that the foregoing automatic tuning methods are merely exemplary and that other *automatic tuning methods* based on the principals disclosed herein may be employed. [McCarthy, 0020]

Furthermore, McCarthy teaches the use of automatic tuning methods for VCOs, which generate frequencies, not for filters, which block certain frequencies. McCarthy's only mention of a filter regards the use of external inductances for higher order filters.

Claims 1-3, 5 and 37-39

Claim 1 is directed toward an intermediate frequency filter for use in an integrated circuit, comprising a first filter stage, the first filter stage including a first LC resonator, and the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface. As discussed above, and admitted to within the Office Action, the combination of Shen and McCarthy do not teach an adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface. Therefore, the combination of Shen and McCarthy does not teach every element of Claim 1. As a result, Claim 1 is allowable over the combination of Shen and McCarthy. Claims 2, 3 and 5 are dependent upon the allowable Claim 1 and are therefore similarly allowable.

Claims 8 and 9

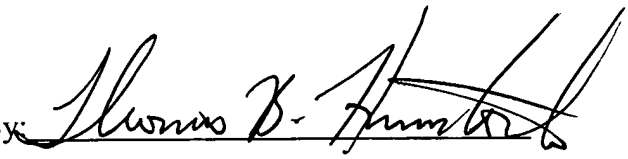
Claim 8 is directed toward a circuit formed as part of a single integrated circuit, the circuit comprising a first amplifier, a first oscillator, a first mixer coupled to the first amplifier and the first oscillator, a second oscillator, a second mixer coupled to the second oscillator, a second amplifier coupled to the second mixer, a serial control module, an intermediate frequency filter (IF filter), the IF filter including a first filter stage, the first filter stage including a first LC resonator, the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of fuses, the first plurality of fuses programmable through the serial control module, and wherein the second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer. As admitted to within the Office Action, and discussed in detail above, the combination of Shen and McCarthy do not teach a circuit having a serial control module or a filter with an adjustable capacitive bank. Furthermore, neither Shen nor McCarthy, either alone or in combination, teaches a filter having an adjustable capacitive bank adjusted by a first set of fuses wherein the fuses are adjustable through a serial control module. Therefore, the combination of Shen and McCarthy do not teach every element of Claim 8. As a result, Claim 8 is allowable over the teachings of Shen and McCarthy. Claim 9 is dependent upon the allowable Claim 8, and is therefore similarly allowable.

Conclusion

The Applicants respectfully submit that the above claims are in a condition for allowance, and allowance at an early date would be appreciated. If the Examiner has any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss them so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 11-23-10

By: 

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